RESEARCH ARTICLE OPEN ACCESS

Verilog Implementation of an Efficient Multiplier Using Vedic Mathematics

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ABSTRACT
In this paper, the design of a 16x16 Vedic multiplier has been proposed using the 16 bit Modified Carry Select Adder and 16 bit Kogge Stone Adder. The Modified Carry Select Adder incorporates the Binary to Excess -1 Converter (BEC) and is known to be the fastest adder as compared to all the conventional adders. The design is implemented using the Verilog Hardware Description Language and tested using the Modelsim simulator. The code is synthesized using the Virtex-7 family with the XC7VX330T device. The Vedic multiplier has applications in Digital Signal Processing, Microprocessors, FIR filters and communication systems. This paper presents a comparison of the results of 16x16 Vedic multiplier using Modified Carry Select Adder and 16x16 Vedic Multiplier using Kogge Stone Adder. The results show that 16x16 Vedic Multiplier using Modified Carry Select Adder is more efficient and has less time delay as compared to the 16x16 Vedic Multiplier using Kogge Stone Adder.

Keywords **-** Binary to Excess -1 Converter (BEC), Kogge Stone adder, Modified Carry Select Adder, Vedic Multiplier

I. INTRODUCTION

The Vedic multiplication technique is an ancient multiplication technique which was rediscovered by Sri Bharati Krishna Tirthaji, between 1911 and 1918 who was a scholar of Sanskrit, Mathematics, Philosophy and History. Due to the ever growing need of a high speed multiplier for the high speed processors there has been a vast development of fast multiplier circuits which have less power consumption, area and less time delay. The multipliers have applications in communication applications, processors, digital signals processing and FIR filters. The Vedic mathematics mainly comprises of the "16 sutras" where these sutras represent the different branches of mathematics like geometry, algebra. The Vedic mathematics reduces the complex calculations into simpler ones. And thus it is more efficient and makes use of less hardware. Therefore, the use of the Vedic multiplication technique the higher throughput arithmetic operations can be achieved which lead to an increased performance in many real time signal and image processing applications.

II. THE URDHVA TIRYAKBHYAM SUTRA

The Vedic multiplier proposed in this paper is based on the "Urdhva Tiryakbhyam" sutra, which means Vertically and Crosswise. This algorithm can be used for binary as well as decimal number multiplication.

The "Urdhva Tiryakbhyam" algorithm is described using two decimal numbers 456 and 642 in Fig 1 which involves the generation of partial products and their summation. In the first stage of multiplication the two digits connected through the line are multiplied. The carry from the previous stage is taken as zero. The first digit of the obtained product is stored as the result's first digit and the other digit of the product is the carry for the next stage. In the second stage again the digits connected through the line are multiplied and their sum is added to the carry of the previous stage. The obtained sum's first digit is stored as the result's second digit and the other digit is the carry for the next stage. This process is repeated until the product of the two decimal numbers is obtained as shown in Fig 1.

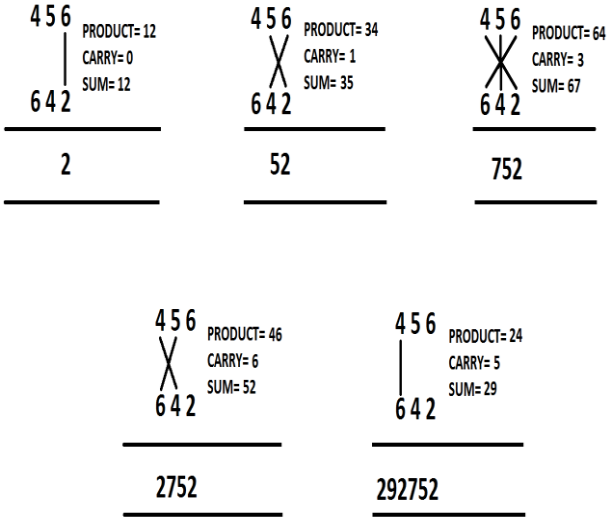

Fig 1. Example of Vedic Multiplication Technique

III. THE MODIFIED CARRY SELECT ADDER

The Modified Carry Select Adder incorporates a Binary to Excess-1 Converter (BEC) which reduces the area and the time delay of this adder and thus, it is a more efficient adder as compared to all other conventional adders. The diagram of Binary to Excess-1 Converter uses the AND, NOT and XOR gate as shown in Fig 2. The final sums of the Modified Carry Select Adder are computed by the help of multiplexers.

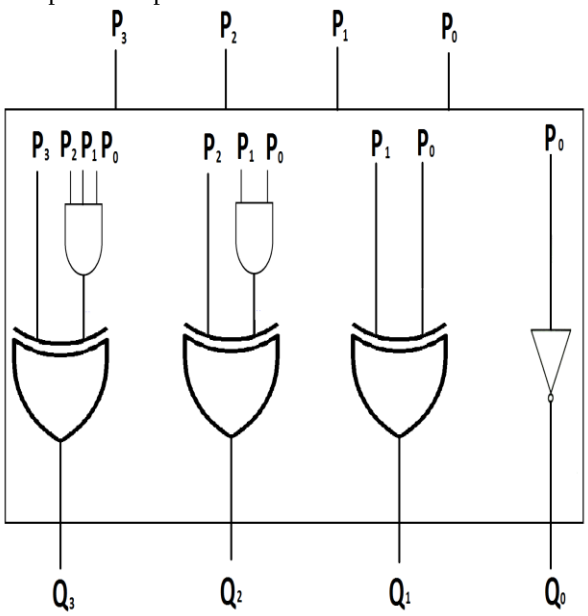

Fig 2. Binary to Excess-1 Converter (BEC)

The logic equations for the Binary to Excess-1 Converter are:

Q 0 =~ P0
Q 1 = P0 ^ P1
Q 2 = P2 ^ (P0 & P1)
Q 3 = P3 ^ (P0 & P1 & P2)

IV. THE KOGGE STONE ADDER

The Kogge Stone Adder can be understood by its three distinct parts: pre-processing, carry look ahead network and post-processing. It is a high performance adder which can generate the carry signal in O (log t) time. It is a parallel prefix form carry look ahead adder. It produces a "propagate" and "generate" in each vertical stage. Its concept was developed by Peter M. Kogge and Harold S. Stone. The functioning of the Kogge Stone Adder is depicted in Fig 3.

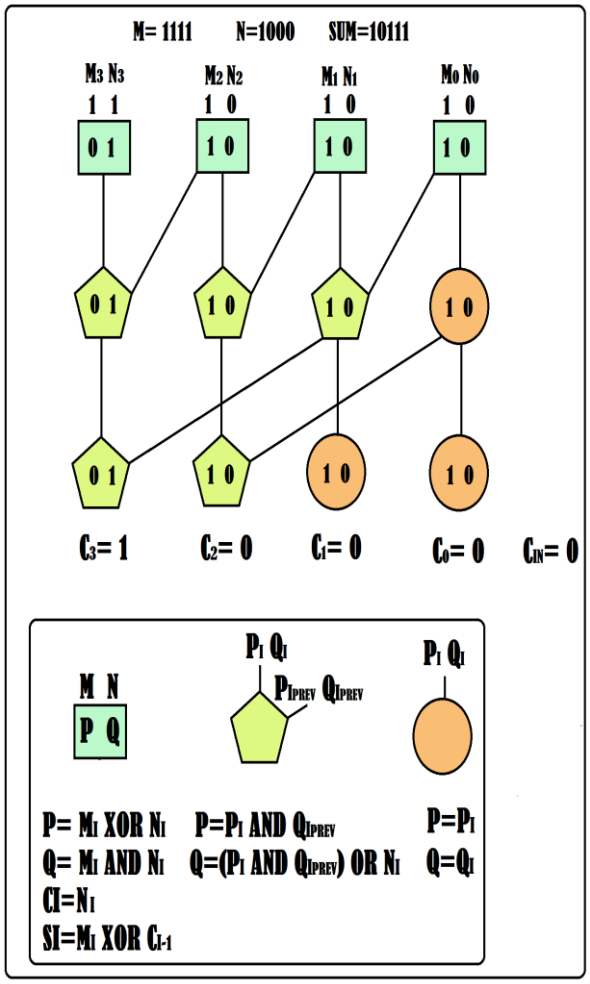

Fig 3. The Kogge Stone Adder

V. 16X16 VEDIC MULTIPLIER USING MODIFIED CARRY SELECT ADDER

The 16 bit Vedic Multiplier using the Modified Carry Select Adder consists of four 8 bit Modified Carry Select Adders for obtaining the product of two 16 bits numbers. The block diagram of this multiplier is shown in Fig 4 where the transfer from each bit from one stage to another stage is shown along with the carry generated in the intermediate stages. The two 16 bit inputs are taken as M [15:0] and N [15:0] and their obtained product is O [31:0] along with the carry C.

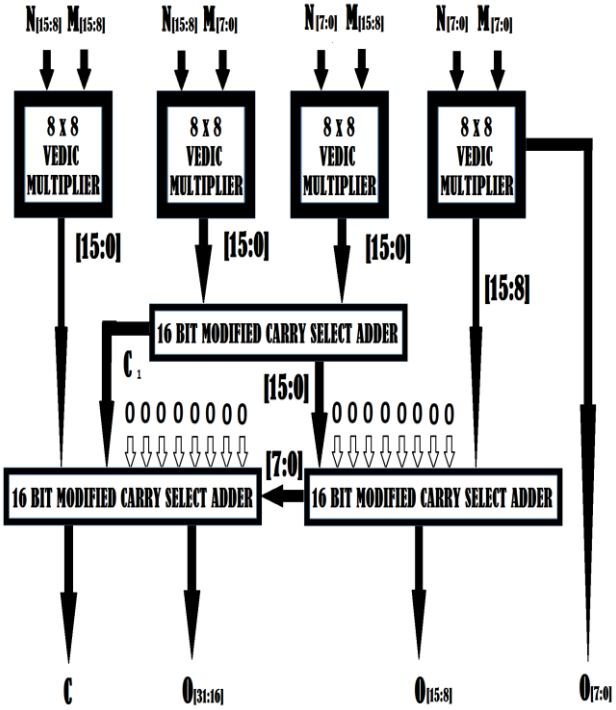

Fig 4. Block Diagram of 16 Bit Vedic Multiplier using Modified Carry Select Adder

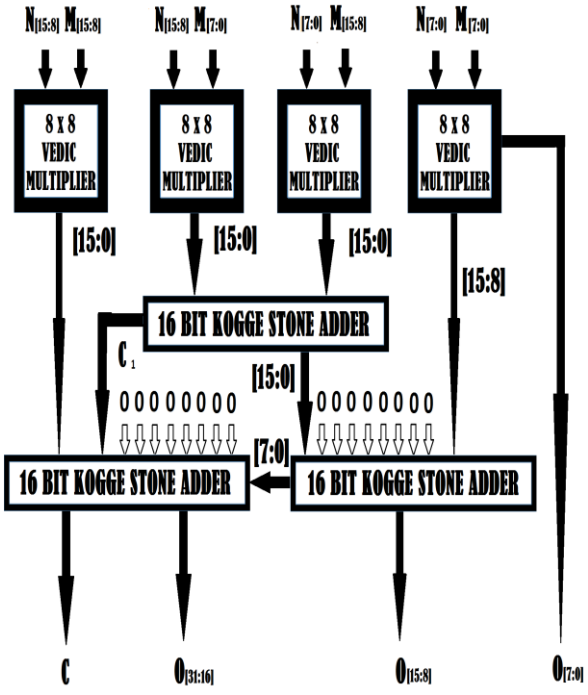

Fig 5. Block Diagram of 16 Bit Vedic Multiplier using Kogge Stone Adder

VI. 16X16 VEDIC MULTIPLIER USING KOGGE STONE ADDER

The 16 bit Vedic multiplier using the Kogge Stone Adder consists of four 8 bit Vedic multipliers and three 16 bit Kogge stone adders for the evaluation of the two 16 bit inputs. The two 16 bit inputs taken are M [15:0] and N [15:0] and their product obtained is O [31:0] along with the carry C. Fig 5 has been shown depicting the block diagram of 16 bit Vedic multiplier using the Kogge stone adder and the transfer of each bit from one stage to another stage has also been shown along with all the internal carry generated.

VII. RESULT

The 16 bit Vedic multiplier using the Modified Carry Select Adder and the 16 bit Vedic multiplier using the Kogge Stone Adder were designed using the Verilog Hardware Description Language and tested using the Modelsim simulator. The Virtex-7 family and XC7VX330T device was used. The Virtex-7 family is ready to deliver a two-fold system performance improvement at 50 percent lower power compared to the previous Virtex-6 family. The comparison of the Number of LUTs, Maximum Combinational Path Delay and Maximum Output Required Time after Clock for the Vedic multiplier using the two adders has been shown in Table 1 and the comparison of the Total Power and Peak Memory Usage has been shown in Table 2 for the Vedic multiplier using the two adders. The results show that the 16 bit Vedic Multiplier using Modified Carry Select Adder uses 34.60 percent less path delay, 38.74 percent less Maximum Output Required Time After Clock and 8.20 percent less power as compared to the 16 bit Vedic Multiplier using Kogge Stone Adder.

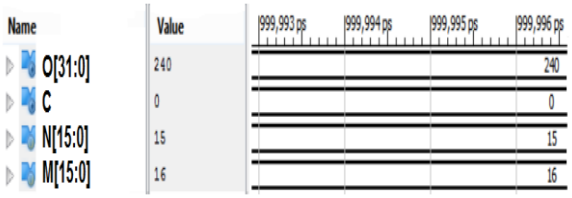

Fig 6. Simulation Result of 16 Bit Vedic Multiplier using Modified Carry Select Adder

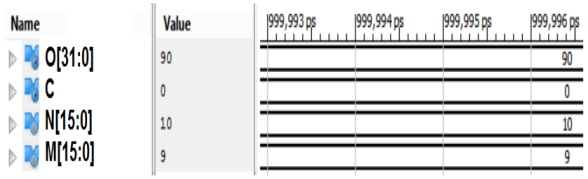

Fig 6. Simulation Result of 16 Bit Vedic Multiplier using Kogge Stone Adder

Vedic Multiplier	No. of Slice LUTs	Maximum Combinational Path Delay (ns)	Maximum Output Required Time After Clock (ns)
Using Modified Carry Select Adder	**21**	**23.367**	**19.236**
Using Kogge Stone Adder	**19**	**35.732**	**31.403**

Table 1. Comparison of Number of Slice LUTs, Maximum Combinational Path Delay and Maximum Output Required Time after Clock.

Vedic Multiplier	Total Power	Peak Memory Usage (MB)
Using Modified Carry Select Adder	**142.92**	**978**
Using Kogge Stone Adder	**155.69**	**998**

Table 2. Comparison of Total Power and Peak Memory Usage.

VIII. CONCLUSION

The 16 bit Vedic multiplier using the Modified Carry Select Adder has less path delay, less peak memory usage and a reduced total power consumption as compared to the 16 bit Vedic multiplier using Kogge Stone Adder. This shows that the 16 bit Vedic multiplier using the Modified Carry Select Adder has an increased speed and less power consumption and can be used in processors for faster computations.

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